



Atty. Dkt. No. 039153-0256 (F0113)

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Yu  
Title: A PROCESS FOR  
MANUFACTURING  
TRANSISTORS HAVING  
SILICON/GERMANIUM CHANNEL  
REGIONS  
Appl. No.: 09/599,141  
Filing Date: 06/22/2000  
Examiner: Roman, A.  
Art Unit: 2812

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| <b>CERTIFICATE OF MAILING</b><br>I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, PO Box 1450, Alexandria, Virginia 22313-1450, on the date below.<br><br>_____<br>(Printed Name)<br><br>_____<br>(Signature)<br>9/2/03<br>_____<br>(Date of Deposit) |
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**SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT**  
**UNDER 37 CFR §1.56**

Commissioner for Patents  
PO Box 1450  
Alexandria, Virginia 22313-1450

Sir:

Submitted herewith on Form PTO-1449 is a listing of documents known to Applicant in order to comply with Applicant's duty of disclosure pursuant to 37 CFR §1.56. A copy of each listed document is being submitted to comply with the provisions of 37 CFR §1.97 and §1.98.

The submission of any document herewith, which is not a statutory bar, is not intended as an admission that such document constitutes prior art against the claims of the present application or that such document is considered material to patentability as defined in 37 CFR §1.56(b). Applicant does not waive any rights to take any action which would be appropriate to antedate or otherwise remove as a competent reference any document which is determined to be a *prima facie* art reference against the claims of the present application.

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**TIMING OF THE DISCLOSURE**

The listed documents are being submitted in compliance with 37 CFR §1.97(c), before the mailing date of either a final action under 37 CFR §1.113, a notice of allowance under 37 CFR §1.113, or an action that otherwise closes prosecution in the application.

**RELEVANCE OF EACH DOCUMENT**

All of the documents are in English.

Applicant respectfully requests that any listed document be considered by the Examiner and be made of record in the present application and that an initialed copy of Form PTO-1449 be returned in accordance with MPEP §609.

**FEE**

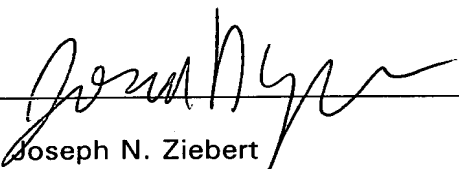
A fee in connection with submission of a supplemental information disclosure statement under 37 CFR §1.97(c) in the amount of \$180.00 in accordance with 37 CFR §1.17(p) is attached.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 CFR §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 06-1447. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 06-1447.

Respectfully submitted,

Date 8-29-03

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PATENT AND TRADEMARK OFFICE

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GROUP ART UNIT

2812

## INFORMATION DISCLOSURE CITATION

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(Use several sheets if necessary)

## U.S. PATENT DOCUMENTS

| EXAMINER<br>INITIAL | REF | DOCUMENT<br>NUMBER | DATE       | NAME              | CLASS | SUB-<br>CLASS | FILING DATE<br>IF<br>APPROPRIATE |
|---------------------|-----|--------------------|------------|-------------------|-------|---------------|----------------------------------|
|                     | A1  | 6,461,945          | 10/8/2002  | Yu                |       |               |                                  |
|                     | A2  | 6,350,311          | 2/26/2002  | Chin et al.       |       |               |                                  |
|                     | A3  | 6,319,799          | 11/20/2001 | Ouyang et al.     |       |               |                                  |
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|                     | A27 | 5,554,870          | 9/10/1996  | Fitch et al.      |       |               |                                  |

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| A39 | 5,036,374 | 7/30/1991  | Shimbo              |  |  |  |
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| REF | DOCUMENT NUMBER | DATE       | COUNTRY  | CLASS | SUB-CLASS | TRANSLATION |    |
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|     |                 |            |          |       |           | YES         | NO |
| A52 | JP-5-335482     | 12/1993    | Japan    |       |           |             |    |
| A53 | EP 0 334 682-A2 | 03/1989    | European |       |           |             |    |
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| Form PTO-1449<br>(MODIFIED)   |     | U.S. DEPARTMENT OF COMMERCE<br>PATENT AND TRADEMARK OFFICE  |  | ATTY. DOCKET NO.<br>039153-0256 (F0113) |  | SERIAL NO.<br>09/599,141 |  |
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| <b>OTHER DOCUMENTS</b> (Including Author, Title, Date, Pertinent Pages, Etc.)   |     |   |  |   |  |                          |  |
|   | A56 | "Sub-100nm Gate Length Metal Gate NMOS Transistors Fabricated by a Replacement Gate Process"<br>By Chatterjee, December 7-10, 1997 IEEE.  |  |   |  |                          |  |
|   | A58 | U.S. Patent Application Serial No. 09/599,270 entitled "A SOLID PHASE EPITAXY PROCESS FOR<br>MANUFACTURING TRANSISTOR SHAVING SILICON/GERMANIUM CHANNEL REGIONS<br>" by Yu on 6/22/00. (Atty. Dkt. No. 39153-268) |  |   |  |                          |  |
|   | A59 | U.S. Patent Application Serial No. 09/817,580 entitled "METHOD OF LOCALLY FORMING A<br>SILICON/GERMANIUM CHANNEL LAYER" by Yu on 03/26/2001. (Atty. Dkt. No. 39153-428)   |  |   |  |                          |  |
|   |     |   |  |   |  |                          |  |
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